EE 2700 Make-up Project
Data Flow Divider

This project is optional and is worth up to half the points you missed on any one mid-term exam.

Design a circuit that performs 8-bit by 8-bit unsigned division. The inputs are an 8-bit dividend and an 8-bit divisor. The outputs are an 8-bit quotient and an 8-bit remainder. If the divisor is 0, the circuit may output anything.

You must model your divider structurally in VHDL. Your design must consist of at least 8 component instances (one per bit). Your components may be behavorial and may use VHDL operators for addition, subtraction or comparison but not multiplication nor division. Loops are not allowed.

Use 8-bit busses for all the inputs and outputs. Give each bus the name given in the table below. Simulate using the test cases given.

Dividend (A)	Divisor (B)	Quotient (Q)	Remainder (R)
255	17	15	0
193	102	1	91
23	3	7	2
149	207	0	149
255	1	255	0
255	2	127	1
255	3	85	0
255	4	63	3
255	5	51	0
255	6	42	3
255	7	36	3

Turn in the top-level (structural) VHDL module along with any other modules you used as components. Also turn in a test-bench and simulation showing the inputs and outputs above. Make sure to set the radix for the inputs and outputs to unsigned decimal so they appear exactly as shown above.

In order to get credit for this assignment, (a) the simulation must be correct and show all the cases above, (b) the top-level module must be structural, (c) no module may contain a loop, and (d) VHDL multiplication and division operators may not be used. Assuming you have done this, you will be given a grade on a scale of 0-50. This percentage will then be multiplied by the number of missed points on your lowest mid-term score. That product (rounded to the nearest integer) will then be added to your score.